Low Level Input Voltage – Table 1

low Level Input voltage in Data Sheet Rev C (Before)

Table 1. (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUT/OUPUT						
Digital Output High Voltage	V_{OH}	SDO pin, load current = −100 µA	$IO_{VCC} - 0.2$			V
Digital Output Low Voltage	V_{OL}	SDO pin, load current = 100 µA			0.2	V
		$\overline{FAULT}$ pin, load current = 100 µA			0.2	V
Digital High-Z Output Leakage Current		SDO pin leakage current ($\overline{CS}$/LD high)	−1		+1	µA
		$\overline{FAULT}$ pin leakage current (not asserted)			1	µA
Digital Input Current		Input voltage (V_{IN}) = GND to IO_{VCC}	−1		+1	µA
Digital Input Capacitance[10]	C_{IN}				8	pF
High Level Input Voltage	V_{IH}	$2.85 \leq IO_{VCC} \leq V_{CC}$	$0.8 \times IO_{VCC}$			V
		$1.71 \leq IO_{VCC} \leq 2.85$	$0.8 \times IO_{VCC}$			V
Low Level Input Voltage	V_{IL}	$2.85 \leq IO_{VCC} \leq V_{CC}$			0.3	V
		$1.71 \leq IO_{VCC} \leq 2.85$			0.3	V

Low Level Input Voltage – Table 1

low Level Input voltage in Data Sheet Rev D (After)

Table 1. (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUT/OUPUT						
Digital Output High Voltage	V_{OH}	SDO pin, load current = −100 µA	IO_{VCC} − 0.2			V
Digital Output Low Voltage	V_{OL}	SDO pin, load current = 100 µA			0.2	V
		$\overline{FAULT}$ pin, load current = 100 µA			0.2	V
Digital High-Z Output Leakage Current		SDO pin leakage current ($\overline{CS}$/LD high)	−1		+1	µA
		$\overline{FAULT}$ pin leakage current (not asserted)			1	µA
Digital Input Current		Input voltage (V_{IN}) = GND to IO_{VCC}	−1		+1	µA
Digital Input Capacitance[10]	C_{IN}				8	pF
High Level Input Voltage	V_{IH}	$2.85 \leq IO_{VCC} \leq V_{CC}$	$0.8 \times IO_{VCC}$			V
		$1.71 \leq IO_{VCC} \leq 2.85$	$0.8 \times IO_{VCC}$			V
Low Level Input Voltage	V_{IL}	$2.85 \leq IO_{VCC} \leq V_{CC}$			0.5	V
		$1.71 \leq IO_{VCC} \leq 2.85$			0.3	V